L Number	Hits	Search Text	DB	Time stamp
2	9365	interconnect same capacitor	USPAT; US-PGPUB	2003/05/06 15:11
3	4233	(interconnect same capacitor) and @ad<=20000818	USPAT; US-PGPUB	2003/05/06 14:51
4	3[illegible]	((interconnect same capacitor) and @ad<=20000818) and (trench or opening or hole or via or recess)	USPAT; US-PGPUB	2003/05/06 15:11
5	3[illegible]	(((interconnect same capacitor) and @ad<=20000818) and (trench or opening or hole or via or recess)) and ((lower or bottom) adj electrode)	USPAT; US-PGPUB	2003/05/06 15:11
6	94[illegible]	interconnect same capacitor	EPO; JPO; DERWENT; IBM_TDB	2003/05/06 15:11
7	311	(interconnect same capacitor) and (trench or opening or hole or via or recess)	EPO; JPO; DERWENT; IBM_TDB	2003/05/06 15:11
8	25	((interconnect same capacitor) and (trench or opening or hole or via or recess)) and ((lower or bottom) adj electrode)	EPO; JPO; DERWENT; IBM_TDB	2003/05/06 15:12

DERWENT-ACC-NO: 2003-055003

DERWENT-WEEK: 200324

TITLE: Method for fabricating metal interconnection and capacitor of semiconductor device

INVENTOR: KIM, S B

PATENT-ASSIGNEE: HYNIX SEMICONDUCTOR INC[HYNIN]

PRIORITY-DATA: 2000KR-0085142 (December 29, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 358050 B	October 25, 2002	N/A	000	H01L 027/108
KR 2002055889 A	July 10, 2002	N/A	001	H01L 027/108

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR 358050B	N/A		
2000KR-0085142	December 29, 2000		
KR 358050B	Previous Publ.	KR2002055889	N/A
KR2002055889A	N/A		
2000KR-0085142	December 29, 2000		

INT-CL (IPC): H01L027/108

ABSTRACTED-PUB-NO: KR2002055889A

BASIC-ABSTRACT:

NOVELTY - A method for fabricating a metal interconnection and a capacitor of a semiconductor device is provided to form a

metal-insulator-metal(MIM)
capacitor capable of being transplanted to a conventional interconnection
formation process, by forming the MIM capacitor of a three-dimensional
structure in a conventional dual damascene pattern.

DETAILED DESCRIPTION - A predetermined region of an interlayer dielectric(2) is
etched to form the dual damascene pattern composed of a **trench or trench/via** in
a semiconductor substrate(1). The first metal diffusion barrier layer(4) and a
copper seed layer are formed on the substrate. A photoresist layer pattern is
formed to expose the first metal diffusion barrier layer and the copper seed
layer on a mask formed on an interlayer between a capacitor formation region(A)
and a metal interconnection region(B). The exposed portion of the first metal
diffusion barrier layer is etched and the photoresist layer pattern is
eliminated. An electroplating metal layer is formed on the first metal
diffusion barrier layer or copper seed layer in the metal interconnection
region. A **lower electrode**(13), a dielectric layer(14), an upper electrode(15)
and the second metal diffusion barrier layer(10) are sequentially formed. A
metal layer for the second metal interconnection(12) is formed to completely
fill the rest of the space of the **trench** or dual damascene pattern. The metal
layer for the second metal interconnection, the second metal diffusion barrier
layer, the upper electrode, the dielectric layer, the **lower electrode** and the
first metal diffusion barrier layer are removed and planarized to form the
second metal interconnection and the capacitor.

CHOSEN-DRAWING: Dwg.1/10

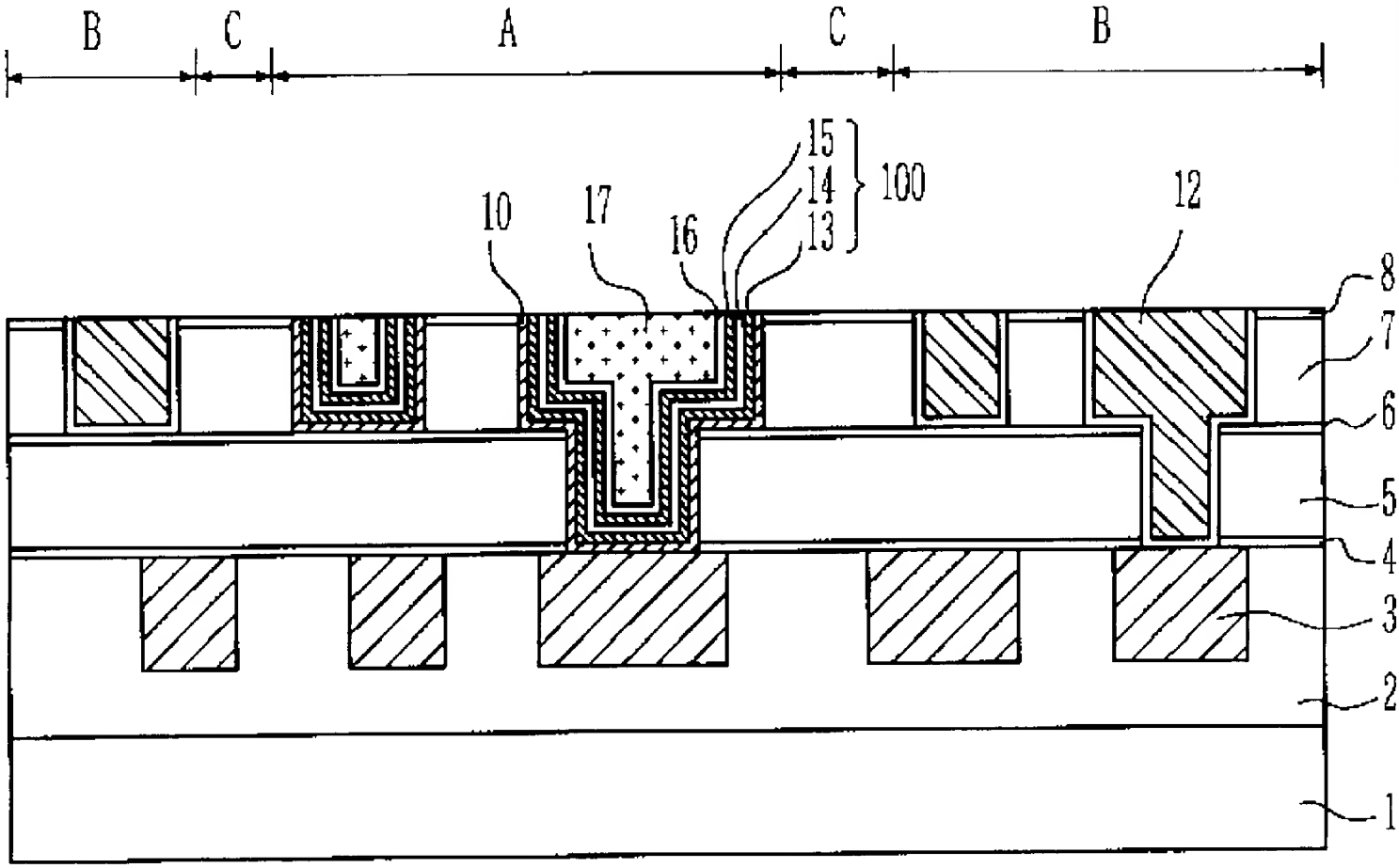
TITLE-TERMS: METHOD FABRICATE METAL **INTERCONNECT CAPACITOR** SEMICONDUCTOR DEVICE

DERWENT-CLASS: L03 U11 U13 U14

CPI-CODES: L04-C13B; L04-C14A;

EPI-CODES: U11-A08B; U13-C04B1A; U14-A03B4;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2003-014322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DERWENT-ACC-NO: 2000-627839

DERWENT-WEEK: 200239

TITLE: Fabrication of embedded dynamic random access memory circuits with logic circuits involves two levels of metals to concurrently form the capacitor and metal interconnections for the logic

INVENTOR: HUANG, J M

PATENT-ASSIGNEE: TAIWAN SEMICONDUCTOR MFG CO[TASEN]

PRIORITY-DATA: 1999US-0372075 (August 11, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 6117725 A	September 12, 2000	N/A	014	H01L 021/8242

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 6117725A	N/A	1999US-0372075	August 11, 1999

INT-CL (IPC): H01L021/8242

RELATED-ACC-NO: 2002-360463

ABSTRACTED-PUB-NO: US 6117725A

BASIC-ABSTRACT:

NOVELTY - An embedded dynamic random access memory (DRAM) circuits with logic

circuits are fabricated by using two levels of metals to concurrently form the
DRAM capacitors and metal interconnections for the logic. The metal layers are
deposited at lower temperatures.

DETAILED DESCRIPTION - An embedded DRAM circuits with logic circuits are
fabricated by forming a planar first insulating layer (20) on the substrate
(10) having logic regions with salicide field-effect transistors (FETs) and
memory regions with device areas. First **openings** (2) in the insulating layer
are etched for contacts to the salicide FETs. An **opening** for bit lines and
capacitor node contacts (19) in the memory region are also concurrently etched.
Metal plugs (30, 38) are formed in the **opening**. A patterned first metal layer
is formed for a first level of metal interconnections (40) including bit lines.
A planar second insulating layer (28) is formed. Second **openings** on and to the
capacitor node contacts are etched. **Via holes** (8) are etched for the salicide
FETs and metal **bottom electrodes** are formed in the second **openings** and metal
contacts. An interelectrode dielectric layer (32) is deposited and patterned
leaving portions on the **bottom electrodes**. A second metal layer (34) is
deposited and patterned to form a second level of interconnections and
concurrently forming capacitor top electrodes.

USE - For fabricating an embedded DRAM circuits with logic circuits.

ADVANTAGE - The invention does not electrically degrade the high performance
salicide field-effect transistors having shallow diffused source/drain
junctions with thin salicide contacts. It provides a plane structure using a
cost-effective process.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view
of the invention.

First **openings** 2

Via holes 8

Substrate 10

Contacts 19

First insulating layer 20

Second insulating layer 28

Metal plugs 30, 38

Second metal layer 34

Dielectric layer 32

Metal interconnections 40

CHOSEN-DRAWING: Dwg.8/8

TITLE-TERMS: FABRICATE EMBED DYNAMIC RANDOM ACCESS MEMORY CIRCUIT LOGIC CIRCUIT
TWO LEVEL METAL CONCURRENT FORM **CAPACITOR** METAL **INTERCONNECT** LOGIC

DERWENT-CLASS: L03 U11 U12 U13 U14

CPI-CODES: L03-G04A; L04-C10; L04-C13B; L04-C14A;

EPI-CODES: U11-C05D4; U11-C05F6; U11-C05G1B; U11-C18B5; U12-C02A1; U12-Q;
U13-C04B1A; U14-A03B4; U14-C01;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2000-188031
Non-CPI Secondary Accession Numbers: N2000-465167